PATENT ABSTRACTS

[your application]

7/5/2 (Item 2 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014884143 & *Drawing available*
WPI Acc no: 2005-231882/200524
XRPX Acc No: N2005-190985
Probabilistic task e.g. orthopedic surgery setting, scheduling method, involves generating cost for each task, based on probabilities of selecting resources for each task, and scheduling task of minimum cost
Patent Assignee: MATHESON E (MATH-I); SHAPIRO M (SHAP-I)
Inventor: MATHESON E; SHAPIRO M

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050055179	A1	20050310	US 2003656355	A	20030905	200524	B

Priority Applications (no., kind, date): US 2003656355 A 20030905

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
US 20050055179	A1	EN	19	7	

Alerting Abstract US A1
NOVELTY - The method involves receiving task containers (204-222) representing set of tasks to be scheduled. The containers describe one or more resources required for the represented task. The container information describes the selection of tasks or resources. A cost for each task is generated based on probabilities of selecting resources for each of the tasks. The minimum cost task is scheduled.
DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

a. a processor readable medium storing instructions for performing scheduling based on probabilities associated with tasks
b. a system for scheduling several tasks.

USE - Used for performing scheduling based on probabilities associated with tasks such as orthopedic surgery setting.
ADVANTAGE - The method solves complex task scheduling problem by scheduling the ask having minimum cost.
DESCRIPTION OF DRAWINGS - The drawing shows a hierarchical arrangement of a main task log, tasks, resource containers, and named resources.
202Main task log
204,206,208,210,212, 214,222Task containers
216,218,220, 226,228,230Resources

13/5/1 (Item 1 from file: 347) Links
Fulltext available through: Order File History
JAPIO

05650605 **Image available**
EXCLUSIVE ACCESS METHOD FOR SHARED RESOURCE

Pub. No.: 09-265405 [JP 9265405 A]
Published: October 07, 1997 (19971007)
Inventor: OGAWA GUNJI
Applicant: FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
Application No.: 08-076414 [JP 9676414]
Filed: March 29, 1996 (19960329)
International Class: [6] G06F-009/46
JAPIO Class: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)

ABSTRACT
PROBLEM TO BE SOLVED: To guarantee exclusive reference and updating to shared resources without affecting other tasks even when an exclusive task is abnormally ended by providing a priority for exclusively accessing the shared resources or the like.

SOLUTION: In the case that the value of the priority 4 at present of a certain execution body 3 (task) is Px, after preserving the Px, the value of the priority 4 is turned to a smallest value P1, re-dispatching is requested to the dispatcher 2 of an OS, (and after temporarily surrendering a CPU execution right,) the priority 4 of the task is changed to a large value and an access right (CPU execution right) to the shared resources is exclusively allocated by the clispatcher 2. Then, the task exclusively accesses the shared resources and executes a processing. At the point of time when the processing is ended, the value of the priority 4 is restored to the preserved original priority Px.

13/5/2 (Item 2 from file: 347) Links
Fulltext available through: Order File History
JAPIO

02924746 **Image available**
CONTROL SYSTEM FOR SHARED MEMORY

Pub. No.: 01-222346 [JP 1222346 A]
Published: September 05, 1989 (19890905)
Inventor: NISHIYAMA TAKATOMO
Applicant: NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
Application No.: 63-048166 [JP 8848166]
Filed: February 29, 1988 (19880229)
International Class: [4] G06F-012/00
JAPIO Class: 45.2 (INFORMATION PROCESSING -- Memory Units)
Journal: Section: P, Section No. 969, Vol. 13, No. 540, Pg. 45, December 05, 1989 (19891205)

ABSTRACT
PURPOSE: To improve the action independence of inter-task and to improve the reliability of a computer system by previously checking an abnormal access to an unallotted memory or release by means of the request from a task and limiting access influence on the other tasks.

CONSTITUTION: A memory control table 2 storing the allotting state of a memory on a shared memory pool and an allotting memory size, and a memory control means 1 which collates the memory control table 2, controls the allotting state of the memory on the shared memory pool in accordance with the request from the task and checks the justification of the reading and writing of data for the memory and the release of the memory are provided. Thus, the malfunction of one task in plural tasks, which is to operate independently in essential, is prevented from causing the malfunction of the other tasks.

13/5/11 (Item 8 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0012479882 & *Drawing available*
WPI Acc no: 2002-426773/200245
XRPX Acc No: N2002-335575
Co-ordinating method for data management operations in a data storage system managed by a set of data management operations concurrently executing by task director first and second data management operations with separate sets of tasks
Patent Assignee: IBM CORP (IBMC); IBM DEUT GMBH (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: ARCHIBALD J E; MCKEAN B D; MCKEEN B D; DENNIS M B

Patent Family (11 patents, 96 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 2002037255	A2	20020510	WO 2001EP11058	A	20010925	200245	B
AU 200215898	A	20020515	AU 200215898	A	20010925	200258	E
KR 2003045842	A	20030611	KR 2003705781	A	20030425	200370	E
JP 2004513423	W	20040430	WO 2001EP11058	A	20010925	200430	E
			JP 2002539940	A	20010925		
CN 1555521	A	20041215	CN 2001818206	A	20010925	200519	E
US 6918006	B1	20050712	US 2000703822	A	20001030	200546	E
AU 2002215898	A8	20051013	AU 2002215898	A	20010925	200611	E
JP 3777156	B2	20060524	WO 2001EP11058	A	20010925	200635	E
			JP 2002539940	A	20010925		
CN 1256656	C	20060517	CN 2001818206	A	20010925	200661	E
KR 546974	B1	20060131	WO 2001EP11058	A	20010925	200682	E
			KR 2003705781	A	20030425		
TW 249703	B1	20060221	TW 2001126385	A	20011025	200716	E

Priority Applications (no., kind, date): US 2000703822 A 20001030

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 2002037255	A2	EN	24	4		
National Designated States,Original	AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ PH PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW					
Regional Designated States,Original	AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZW					
AU 200215898	A	EN			Based on OPI patent	WO 2002037255
JP 2004513423	W	JA	41		PCT Application	WO 2001EP11058
					Based on OPI patent	WO 2002037255
AU 2002215898	A8	EN			Based on OPI patent	WO 2002037255
JP 3777156	B2	JA	13		PCT Application	WO 2001EP11058
					Previously issued patent	JP 2004513423
					Based on OPI patent	WO 2002037255
KR 546974	B1	KO			PCT Application	WO 2001EP11058
					Based on OPI patent	WO 2002037255
TW 249703	B1	ZH				

Alerting Abstract WO A2

NOVELTY - The method involves concurrently executing, by a task director, first and second data management operations. The first operation has a first set of tasks and the second operation has a second set of tasks. The task director controls the execution or the non-execution of each task of the two sets of tasks based on a set of predetermined rules.

DESCRIPTION - In the step of executing, the first operation is a different operation a compared to the second operation.

INDEPENDENT CLAIMS are included for a data storage system, for a management device and for a computer program product.

USE - For data storage systems.

ADVANTAGE - Provides for concurrently executing data management operations. Reduces time and system resources required for data management operations.

DESCRIPTION OF DRAWINGS - The figure shows a system for co-ordinating data management operations.

13/5/23 (Item 20 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0007414515 & & *Drawing available*
WPI Acc no: 1996-022047/199603
XRPX Acc No: N1996-018301
Hierarchical resource management method for time-sharing OS - involves linking resource management processes into groups on parent-child basis according to management tree using resources from parent resource group
Patent Assignee: NEC CORP (NIDE)
Inventor: SHIMAMURA N

Patent Family (5 patents, 4 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
EP 686915	A2	19951213	EP 1995108015	A	19950524	199603	B
JP 7319715	A	19951208	JP 1994138330	A	19940527	199607	E
US 5682530	A	19971028	US 1995450783	A	19950525	199749	E
EP 686915	B1	20010808	EP 1995108015	A	19950524	200146	E
DE 69522046	E	20010913	DE 69522046	A	19950524	200161	E
			EP 1995108015	A	19950524		

Priority Applications (no., kind, date): JP 1994138330 A 19940527

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
EP 686915	A2	EN	22	8		
Regional Designated States,Original	DE FR GB					
JP 7319715	A	JA	9			
US 5682530	A	EN	18	8		
EP 686915	B1	EN				
Regional Designated States,Original	DE FR GB					
DE 69522046	E	DE			Application	EP 1995108015
					Based on OPI patent	EP 686915

Alerting Abstract EP A2
The management method involves hierarchically forming resource management groups including several processes. Each group includes a resource management process (20, 50 and 80) managing the resources allocated to the group. One process is a descendant of the resource management process and is not included in other groups and acts as a resource management block storing information on the resources managed by its own group.
Resource management processes are linked to each other in accordance with parent-child relationships between the groups to form a resource management tree (100). When a new group is generated, resources necessary for the new group are distributed from resources owned by a parent resource group of the new one in accordance with the management tree.
ADVANTAGE - Ensures execution of each job without being dependent on process operating in other resource management group and affecting that process. Hierarchically manages system resources for use on job basis in advance.

18/5/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0014318979 & & *Drawing available*
WPI Acc no: 2004-506395/200448
XRPX Acc No: N2004-400086
Computer system for processing client requests, has grid services scheduler that divides client request into several tasks and assigns them to micro schedulers which is turn assign tasks to objects of persistent containers
Patent Assignee: CHALLENGER J R H (CHAL-I); IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC); NOVAES M (NOVA-I)
Inventor: CHALLENGER J R H; NOVAES M

Patent Family (3 patents, 3 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20040123296	A1	20040624	US 2002328255	A	20021223	200448	B
JP 2004206712	A	20040722	JP 2003421634	A	20031218	200448	E
CN 1516419	A	20040728	CN 200310121564	A	20031222	200469	E

Priority Applications (no., kind, date): US 2002328255 A 20021223

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20040123296	A1	EN	22	8		
JP 2004206712	A	JA	26			

Alerting Abstract US A1
NOVELTY - A topology aware grid services scheduler (TAGSS) is connected to several grid container arrays comprising several persistent containers residing in host computer and micro scheduler. The TAGSS divides a client request into several tasks and assigns them to each micro scheduler which is turn assign the tasks to objects of containers within corresponding grid object array.
DESCRIPTION - An INDEPENDENT CLAIM is also included for method for processing client requests over computer network of hosts.
USE - Computer system for processing client requests, using scheduler e.g. topology aware grid services scheduler (TAGSS) over computer network, in diverse computing environment for handling large amount of data.
ADVANTAGE - By using the TAGSS that divides client request into several tasks in real time, multiple client requests can be processed effectively.
DESCRIPTION OF DRAWINGS - The figure shows a schematic view illustrating the process of creating containers on demand.

18/5/2 (Item 2 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0009410446 & & *Drawing available*
WPI Acc no: 1999-347328/199929
Related WPI Acc No: 2001-257649; 2001-580000; 2002-528261
XRPX Acc No: N1999-259698
Modular healthcare information management system
Patent Assignee: DEROYAL BUSINESS SYSTEMS LLC (DERO-N); DEROYAL IND INC (DERO-N)
Inventor: COFER M C; DEBUSK B C; LUKENS W F; SHANKS M W

Patent Family (4 patents, 21 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
WO 1999024927	A1	19990520	WO 1998US23592	A	19981105	199929	B
US 5995937	A	19991130	US 1997965788	A	19971107	200003	E
EP 1029301	A1	20000823	EP 1998957610	A	19981105	200041	E
			WO 1998US23592	A	19981105		
JP 2002512389	W	20020423	WO 1998US23592	A	19981105	200243	E
			JP 2000519852	A	19981105		

Priority Applications (no., kind, date): US 1997965788 A 19971107

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
WO 1999024927	A1	EN	47	2		
National Designated States,Original	CA JP					
Regional Designated States,Original	AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE					
EP 1029301	A1	EN			PCT Application	WO 1998US23592
					Based on OPI patent	WO 1999024927
Regional Designated States,Original	DE ES FR GB IT NL SE					
JP 2002512389	W	JA	42		PCT Application	WO 1998US23592
					Based on OPI patent	WO 1999024927

Alerting Abstract WO A1
NOVELTY - Each node (200) provides a particular information management function and represents a software object allowing a user to perform certain functions and tasks. Container objects (204), resource objects (206) and data objects (208) are available to a user. The container objects act to organize the objects, the resource objects represent resources to be utilized in provision of health care and the data objects are software used to collect specific information for use by templates or an information system
USE - Supplying, scheduling and managing in healthcare environment
ADVANTAGE - Providing integrated information system utilizing modular component software structure
DESCRIPTION OF DRAWINGS - The drawing is a block diagram showing generic form of present invention
200 Nodes
204 Container objects
206 Resource objects
208 Data objects

18/5/3 (Item 3 from file: 350) Links
Fulltext available through: Order File History
Derwent WPIX

0008095094
WPI Acc no: 1997-192392/199717
Related WPI Acc No: 1994-218083; 1997-033851; 1997-297648; 1998-311631; 1998-494995
XRPX Acc No: N1997-158997
Interacting with containee object within container object for linked and embedded objects for spreadsheet application - determining whether to invoke container application code or server application code and executing server application code as separately scheduled entity to process server resource selection when selected resource is server resource
Patent Assignee: MICROSOFT CORP (MICR-N)
Inventor: HODGES C D; KOPPOLU S R; MACKICHAN B B; MCDANIEL R; REMALA R V; WILLIAMS A S

Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 5613058	A	19970318	US 1992984868	A	19921201	199717	B
			US 1994229264	A	19940415		

Priority Applications (no., kind, date): US 1992984868 A 19921201; US 1994229264 A 19940415

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 5613058	A	EN	97		C-I-P of application	US 1992984868

Alerting Abstract US A
The container object has a container application with a container window environment that has container resources for interacting with the container object. The containee object has a server application with a server window environment with server resources for interacting with the containee object.
The container window environment is displayed on a display. A user then selects the containee object. In response to selecting the containee object, the server resources are integrated with the displayed container window environment. When a user then selects a server resource, the server application is invoked to process the server resource selection. Conversely, when a user selects a container resource, the container application is invoked to process the container resource selection.

8/3K/3 (Item 1 from file: 349) Links
Fulltext available through: Order File History

00507933
SYSTEM AND METHOD FOR CREATING AND MANIPULATING INFORMATION CONTAINERS WITH DYNAMIC REGISTERS
SYSTEME ET PROCEDE POUR LA CREATION ET LA MANIPULATION DE CONTENEURS D'INFORMATIONS A REGISTRES DYNAMIQUES

Patent Applicant/Patent Assignee:

c. EMATRIX CORPORATION;
; ;

d. DE ANGELO Michael;
; ;

	Country	Number	Kind	Date
Patent	WO	9939285	A1	19990805
Application	WO	99US1988		19990128
Priorities	US	9873209		19980130

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

Main International Patent Classes (Version 7):

IPC	Level
G06F-017/30	Main
G06F-003/14	

Publication Language: English
Filing Language:
Fulltext word count: 18390

Detailed Description:

...passively, assigning the space, characteristics by which that content will be acted upon by another container or process, and neutrally, assigning the space characteristics by which that container will interact with another container or process, (4) a domain of influence register, determining the set, class and range of containers upon which that container will act...112000 assigning the space, characteristics by which that content will be acted upon by another container or process, and 113000 assigning the space characteristics by which that container will interact with another container or process, a domain of influence register 119000, determining the set, class and range of containers upon which that container will...

11/3K/2 (Item 2 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

00747354
Capability engine method and apparatus for a microkernel data processing system
Verfahren und Gerat mit Fahigkeitsvorrichtung fur ein Mikrokern-Datenverarbeitungssystem
Methode et appareil a dispositif de capacite pour un systeme de traitement de donnees a micro-noyaux

Patent Assignee:

e. International Business Machines Corporation; (200120)
Old Orchard Road; Armonk, N.Y. 10504; (US)
(Proprietor designated states: all)

Inventor:

f. Magee, James Michael
5310 Canal Drive; Lake Worth, Florida 33463; (US)

g. Sotomayor, Guy Gil, Jr.
6042 Sherwood Glen Way, Apt. 3; West Palm Beach, Florida 33415; (US)

h. Youngworth, Christopher Dean
3 Gulfview Court; Savoy, Illinois 61874; (US)

Legal Representative:

i. Williams, Julian David (75461)
IBM United Kingdom Limited, Intellectual Property Department, Hursley Park; Winchester, Hampshire SO21 2JN; (GB)

	Country	Number	Kind	Date	
Patent	EP	704796	A2	19960403	(Basic)
	EP	704796	A3	19980701	
	EP	704796	B1	20000419	
Application	EP	95304188		19950616	
Priorities	US	263313		19940928	

Designated States:
AT; BE; CH; DE; ES; FR; GB; IT; LI; NL;
SE;

International Patent Class (V7): G06F-009/46Abstract Word Count: 141
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200016	1721
CLAIMS B	(German)	200016	1710
CLAIMS B	(French)	200016	1919
SPEC B	(English)	200016	37863
Total Word Count (Document A) 0			

Total Word Count (Document B) 43213
Total Word Count (All Documents) 43213

Specification: ...processing system, that has greater flexibility in the exchange of messages between tasks within a shared memory environment and between distributed data processors that do not share a common memory.

A preferred embodiment of the present invention provides a method and subsystem for interprocess communication in a microkernel architecture data processing system. The data processing system can be a shared memory multiprocessing system or a uniprocessor system. A microkernel operating system is loaded into the memory...engine module that manages capabilities or rights to map regions of the memory. A first task container is formed by the microkernel in the memory, having a set of attributes defining a... ...a memory object, the first set of port rights conferring a capability on the first task container to access the memory object. A second task container is formed in the memory having.... ...selectively enable a transfer of the pointer and the first port rights from the first task container to the second task container to confer onto the second task container the capability to access the memory object. In this manner, the capability engine manages the... ...the Microkernel System, in a fast and efficient manner.

The present invention applies to uniprocessors, shared memory multiprocessors, and multiple computers in a distributed processor system.

Preferred embodiments of the present invention...registration module 500, the asynchronous reply module 600, the transmission control separation module 700, the shared memory support module 800, and the fast path module 900. All of these modules provide services contributing to the interprocess communications operations of the IPC 122.

The microkernel 120 forms two task containers 210 and 210', two threads 248 and 248' that belong to the respective tasks, and... ...210 is created with a pointer 240 that maps the data object 242 into the task container 210. The port rights of the task container 210 enable it to use the pointer 240 to refer to the address space occupied... ...enable a transfer of the pointer 240 and the first port rights from the first task container 210 to the second task container 210' to confer onto the second task container 210' the capability to access the memory object 242. In this manner, the capability engine... ...the Microkernel System 115, in a fast and efficient manner.

The invention applies to uniprocessors, shared memory multiprocessors, and multiple computers in a distributed processor system. Figure 8 shows a functional block...

Claims: ...first task container (210) to said second task container (210') to confer onto said second task container said capability to access said memory object (242);

receiving an asynchronous message from said first task container (210) including said pointer (240) and said first port rights, and handling saidasynchronous message in an asynchronous mode;

alternately receiving a synchronous message from said first task container (210) including said pointer (240) and said first port rights, and handling said synchronous message in a synchronous mode; and

transferring said pointer (242) from said first task container (210) to said second task container (210').

2. A method as claimed in claim 1, wherein said data processing system comprises a shared memory multiprocessor system including a first and a second processor; and wherein

said first task container has a thread that runs on said first processor; and

said second task container has a thread that runs on said second processor and the enabling step enables said... ...from said first task container to said second task container to confer onto said second task container said capability to access said memory object;

said capability engine (300) receiving an asynchronous ...memory of said first processor, said first microkernel including a capability engine module;

a first task container in said memory having a set of attributes defining a first communication port and a... ...a memory object, said first set of port rights conferring a capability on said first task container to access said memory object, said first task container having a thread that runs on said first processor;

an I/O processor sharing said memory with said first processor, and coupled by said communications link with said second processor;

a second task container in said memory having a set of attributes defining a second communication port and a second set of port rights, said second task container having a thread that runs on said I/O communications processor; capability engine registering said first set of port rights for said first task container and said second set of port rights for said second task container; said capability engine comparing said first set of port rights and said second set of...

11/3K/3 (Item 3 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

00730451
Temporary data method and apparatus for a microkernel data processing system
Verfahren und Gerat mit temporaren Daten fur ein Mikrokernendatenverarbeitungssystem
Methode et appareil a donnees temporaires pour un systeme de traitement de donnees a micro-noyaux

Patent Assignee:

j. International Business Machines Corporation; (200120)
Old Orchard Road; Armonk, N.Y. 10504; (US)
(applicant designated states: DE;FR;GB)

Inventor:

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l. Green, Joseph William
301 Norwood Terrace No. 129; Boca Raton, Florida 33431-6588; (US)

m. Magee, James Michael
5310 Canal Drive; Lake Worth, Florida 33463; (US)

n. Youngworth, Christopher Dean
3 Gulfview Court; Savoy, Illinois 61874; (US)

Legal Representative:

o. Williams, Julian David (75461)
IBM United Kingdom Limited, Intellectual Property Department, Hursley Park; Winchester, Hampshire SO21 2JN; (GB)

	Country	Number	Kind	Date	
Patent	EP	689138	A2	19951227	(Basic)
	EP	689138	A3	19980204	
Application	EP	95304172		19950616	
Priorities	US	263633		19940622	

Designated States:
DE; FR; GB;

International Patent Class (V7): G06F-009/46; ; Abstract Word Count: 208

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	EPAB96	602
SPEC A	(English)	EPAB96	40470
Total Word Count (Document A) 41072			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 41072			

Specification: ...registration module 500, the asynchronous reply module 600, the transmission control separation module 700, the shared memory support module 800, and the fast path module 900. All of these modules provide services contributing to the interprocess communications operations of the IPC 122.

The microkernel 120 forms two task containers 210 and 210', two threads 248 and 248' that belong to the respective tasks, and... ...210 is created with a pointer 240 that maps the data object 242 into the task container 210. The port rights of the task container 210 enable it to use the pointer 240 to refer to the address space occupied... ...enable a transfer of the pointer 240 and the first port rights from the first task container 210 to the second task container 210' to confer onto the second task container 210' the capability to access the memory object 242. In this manner, the capability engine... ...the Microkernel System 115, in a fast and efficient manner.

The invention applies to uniprocessors, shared memory multiprocessors, and multiple computers in a distributed processor system. Figure 8 shows a functional block...

19/3K/1 (Item 1 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01402509
An information processing apparatus
Informationsverarbeitungsvorrichtung
Dispositif de traitement d'information

Patent Assignee:

p. Hitachi, Ltd.; (204145)
6 Kanda Surugadai 4-chome; Chiyoda-ku, Tokyo 101-8010; (JP)
(Applicant designated States: all)

q. Xanavi Informatics Corporation; (1813723)
6-35, Hironodai 2-chome; Zama-shi, Kanagawa 228-0012; (JP)
(Applicant designated States: all)

Inventor:

r. Endo, Yoshinori, Hitachi Ltd. Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

s. Okude, Mariko, Hitachi Ltd. Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

t. Hiroshige, Hideo, Hitachi Ltd. Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

u. Nakamura, Kozo, Hitachi Ltd. Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

v. Kawamata, Yukihiro, Hitachi Ltd.Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

w. Yamaashi, Kimiya, Hitachi Ltd. Intell Prop. Group
New Marunouchi Bldg., 5-1, Marunouchi 1-chome; Chiyoda-ku, Tokyo 100-8220; (JP)

Legal Representative:

x. Beetz & Partner Patentanwalte (100712)
Steinsdorfstrasse 10; 80538 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	1187018	A2	20020313	(Basic)
	EP	1187018	A3	20050126	
Application	EP	2001104524		20010302	
Priorities	JP	200057810		20000302	

Designated States:
DE; FR; GB;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-009/46; G01S-005/14; G06F-009/46... Abstract Word Count: 126
NOTE: 3
NOTE: Figure number on first page: 3

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200211	909
SPEC A	(English)	200211	11090
Total Word Count (Document A) 11999			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 11999			

Specification: ...transmitted through the inter-OS message communication when registering the information in the inter-OS shared memory or referring thereto (step 1007). The task to be registered here may be a single task or a plural tasks. Thereafter, the task competes its shared-object creating operation.

Explanation has been made in connection with the arrangement wherein the task of...

19/3K/6 (Item 6 from file: 348) Links
Fulltext available through: Order File History

01258322
METHOD AND SYSTEM FOR REGULATING BACKGROUND TASKS USING PERFORMANCE MEASUREMENTS
VERFAHREN UND SYSTEM ZUM REGELN VON HINTERGRUNDPROZESSEN MIT LEISTUNGSMESSDATEN
PROCEDE ET SYSTEME PERMETTANT DE REGULER LES TACHES D'ARRIERE-PLAN A L'AIDE DE MESURES DE PERFORMANCE

Patent Assignee:

y. MICROSOFT CORPORATION; (749866)
One Microsoft Way; Redmond, WA 98052; (US)
(Proprietor designated states: all)

Inventor:

z. DOUCEUR, John, R.
14705 N.E. 16th Street; Bellevue, WA 98007; (US)

aa. BOLOSKY, William, J.
24622 S.E. Mirrormont Drive; Issaquah, WA 98027; (US)

Legal Representative:

bb. Grunecker, Kinkeldey, Stockmair & Schwanhausser Anwaltssozietat (100721)
Maximilianstrasse 58; 80538 Munchen; (DE)

	Country	Number	Kind	Date	
Patent	EP	1196848	A1	20020417	(Basic)
	EP	1196848	B1	20060412	
	WO	2001006362		20010125	
Application	EP	2000948634		20000712	
	WO	2000US18989		20000712	
Priorities	US	354970		19990716	

Designated States:
AT; BE; CH; CY; DE; DK; ES; FI; FR; GB;
GR; IE; IT; LI; LU; MC; NL; PT; SE;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-009/46; G06F-009/46

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G06F-0009/46	A	I	F	B	20060101	20010130	H	EP
G06F-0009/46	A	I	F	B	20060101	20010130	H	EP

NOTE: No A-document published by EPO

Type	Pub. Date	Kind	Text

Publication: English

Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200615	1019
CLAIMS B	(German)	200615	963
CLAIMS B	(French)	200615	1207
SPEC B	(English)	200615	8432
Total Word Count (Document A) 0			
Total Word Count (Document B) 11621			
Total Word Count (All Documents) 11621			

Specification: ...single process may include more than one background task. However, if multiple tasks use a common resource, then the operation of one task may interfere with the performance of another task, leading the other task to incorrectly suspend its operation. This may lead to unfair measurements, instability, and moreover, two...

19/3K/10 (Item 10 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

00961678
Method for managing a shared memory
Verfahren zum Verwalten eines geteilten Speichers
Procede de gestion d'une memoire partagee

Patent Assignee:

cc. ALCATEL; (201874)
54, rue La Boetie; 75008 Paris; (FR)
(Proprietor designated states: all)

Inventor:

dd. Jouenne, Franck
24 avenue Saint Pierre; 94420 Le Plessis Trevise; (FR)

ee. Guidot, Dominique
15 rue Bernard Palissy; 92310 Sevres; (FR)

ff. Paul Dubois Taine, Benoit
29 rue de la Fontaine Grelot; 92340 Bourg La Reine; (FR)

Legal Representative:

gg. Sciaux, Edmond et al (58919)
Compagnie Financiere Alcatel Departement de Propriete Industrielle, 5, rue Noel Pons; 92734 Nanterre Cedex; (FR)

	Country	Number	Kind	Date	
Patent	EP	872796	A1	19981021	(Basic)
	EP	872796	B1	20040324	
Application	EP	98400941		19980416	
Priorities	FR	974744		19970417	

Designated States:
AT; BE; CH; DE; ES; FR; GB; IT; LI; NL;
PT; SE;

International Patent Class (V7): G06F-009/46; G06F-009/46Abstract Word Count: 51
NOTE: 1
NOTE: Figure number on first page: 1

Type	Pub. Date	Kind	Text

Publication: French
Procedural: French
Application: French

Available Text	Language	Update	Word Count
CLAIMS A	(French)	199843	976
SPEC A	(French)	199843	4485
CLAIMS B	(English)	200413	1032
CLAIMS B	(German)	200413	976
CLAIMS B	(French)	200413	985
SPEC B	(French)	200413	4496

Total Word Count (Document A) 5463
Total Word Count (Document B) 7489
Total Word Count (All Documents) 12952

Claims: ...B1

1. A method of managing data in a shared memory, data contained in the memory being shared by various competing processes, each process generally being constituted by a plurality of competing tasks; said method being characterized in that:

(not within a transaction,

- for each variable to be...

19/3K/13 (Item 13 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

00656365
SHARED LIBRARY LOCATING SYSTEM AND METHOD
SYSTEM UND METHODE ZUR LOKALISIERUNG VON GETEILTEN BIBLIOTHEKEN
SYSTEME ET METHODE DE LOCALISATION DE BIBLIOTHEQUE PARTAGEE

Patent Assignee:

hh. TALIGENT, INC.; (1821850)
10201 N. De Anza Boulevard; Cupertino, CA 95014; (US)
(applicant designated states: DE;FR;GB;IT)

Inventor:

ii. HENINGER, Andrew, G.
1611 Vorte Via; Los Altos, CA 94024; (US)

jj. NAKANO, Russell, T.
1326 Alridge Drive; Sunnyvale, CA 94087; (US)

Legal Representative:

kk. Kindermann, Manfred (6412)
Patentanwalt, Sperberweg 29; D-71032 Boblingen; (DE)

	Country	Number	Kind	Date	
Patent	EP	679273	A1	19951102	(Basic)
	EP	679273	B1	19960821	
	WO	9423360		19941013	
Application	EP	94907138		19940103	
	WO	94US53		19940103	
Priorities	US	42959		19930405	

Designated States:
DE; FR; GB; IT;

International Patent Class (V7): G06F-009/44; ; ; G06F-009/44
NOTE: No A-document published by EPO

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPAB96	1057
CLAIMS B	(German)	EPAB96	1047
CLAIMS B	(French)	EPAB96	1137
SPEC B	(English)	EPAB96	5068
Total Word Count (Document A) 0			
Total Word Count (Document B) 8309			
Total Word Count (All Documents) 8309			

Specification: ...or a system search object. This restriction follows since a search object is a global resource that is shared by all tasks of a team. Permitting removal of a team search object with respect to

one task would adversely affect another task that is dependent upon the search object. For instance, suppose two independent tasks ("task 1...

22/3K/9 (Item 9 from file: 348) Links
Fulltext available through: Order File History
EUROPEAN PATENTS

01563900
Method and apparatus for partitioning resources within a computer system
Verfahren und Vorrichtung zur Betriebsmittelaufteilung in einem Rechnersystem
Procede et dispositif pour partitionner des ressources dans un systeme d'ordinateur

Patent Assignee:

ll. SUN MICROSYSTEMS, INC.; (2616592)
4150 Network Circle; Santa Clara, California 95054; (US)
(Applicant designated States: all)

Inventor:

mm. Hahn, Stephen C.
1860 Harding Avenue; Redwood City, CA 94062; (US)

nn. Marsland, Tim P.
348 Granelli Avenue; Half Moon Bay, CA; (US)

Legal Representative:

oo. Davies, Simon Robert et al (75453)
D Young & Co 120 Holborn; London, EC1N 2DY; (GB)

	Country	Number	Kind	Date	
Patent	EP	1300766	A2	20030409	(Basic)
	EP	1300766	A3	20070228	
Application	EP	2002256574		20020923	
Priorities	US	964148		20010925	

Designated States:
AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; IE; IT; LI; LU; MC; NL;
PT; SE; SK; TR;

Extended Designated States:
AL; LT; LV; MK; RO; SI;

International Patent Class (V7): G06F-009/50; G06F-009/50

IPC	Level	Value	Position	Status	Version	Action	Source	Office
G06F-0009/50	A	I	F	B	20060101	20030210	H	EP
G06F-0009/50	A	I	F	B	20060101	20030210	H	EP

Abstract Word Count: 207
NOTE: 2
NOTE: Figure number on first page: 2

Type	Pub. Date	Kind	Text

Publication: English
Procedural: English
Application: English

Available Text	Language	Update	Word Count
CLAIMS A	(English)	200315	1115

SPEC A	(English)	200315	2948
Total Word Count (Document A) 4064			
Total Word Count (Document B) 0			
Total Word Count (All Documents) 4064			

Specification: ...operating systems have developed a mechanism for assembling a group of resources into a fixed "container" that processes can bind to in order to access the resources. However, resources within a fixed container... ...flexibly changed over time to accommodate changing resource requirements for the various system workloads. Furthermore, resources cannot be shared between containers. Summary of the Invention

Accordingly, one embodiment of the present invention provides a...

[bad date?]

22/3K/12 (Item 1 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

0115370I
COOPERATIVE, SIMULTANEOUS OPERATION ON DATA BY MANY PROCESSES, WITH CONCURRENT RETENTION OF PROCESS STATUS, RESUMED PROCESSING, AND MINIMAL CONSUMPTION OF INTER-NODAL THROUGHPUT
OPERATION COOPERATIVE SIMULTANEE SUR DES DONNEES AU MOYEN DE PLUSIEURS PROCEDES, AVEC CONSERVATION CONCURRENTE DU STATUT DU PROCEDE, TRAITEMENT REPRIS ET CONSOMMATION MINIMALE DE DEBIT INTER-NODAL

Patent Applicant/Patent Assignee:

pp. ADVANCE INFORMATION SYSTEMS; 499 Northwest Bonanza Street, Sumpter, OR 97877
US; US(Residence); US(Nationality)
(For all designated states except: US)

qq. MONTAGNE Michael D; 499 Northwest Bonanza Street, Sumpter, OR 97877
US; US(Residence); US(Nationality)
(Designated only for: US)

Patent Applicant/Inventor:

rr. MONTAGNE Michael D
499 Northwest Bonanza Street, Sumpter, OR 97877; US; US(Residence); US(Nationality);
(Designated only for: US)

Legal Representative:

ss. LABARRE James A(et al)(agent)
Burns, Doane, Swecker & Mathis, LLP, PO Box 1404, Alexandria, VA 22313-1404; US;

	Country	Number	Kind	Date
Patent	WO	200475013	A2-A3	20040902
Application	WO	2004US4532		20040213
Priorities	US	2003447292		20030214
	US	2003748194		20031231

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)
AE; AG; AL; AM; AT; AU; AZ; BA; BB; BG;
BR; BW; BY; BZ; CA; CH; CN; CO; CR; CU;
CZ; DE; DK; DM; DZ; EC; EE; EG; ES; FI;
GB; GD; GE; GH; GM; HR; HU; ID; IL; IN;
IS; JP; KE; KG; KP; KR; KZ; LC; LK; LR;
LS; LT; LU; LV; MA; MD; MG; MK; MN; MW;
MX; MZ; NA; NI; NO; NZ; OM; PG; PH; PL;
PT; RO; RU; SC; SD; SE; SG; SK; SL; SY;
TJ; TM; TN; TR; TT; TZ; UA; UG; US; UZ;
VC; VN; YU; ZA; ZM; ZW;

[EP] AT; BE; BG; CH; CY; CZ; DE; DK; EE; ES;
FI; FR; GB; GR; HU; IE; IT; LU; MC; NL;

PT; RO; SE; SI; SK; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GQ; GW;
ML; MR; NE; SN; TD; TG;

[AP] BW; GH; GM; KE; LS; MW; MZ; SD; SL; SZ;
TZ; UG; ZM; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Main International Patent Classes (Version 7):

IPC	Level
G06F-017/30	Main

Publication Language: English
Filing Language: English
Fulltext word count: 45213

Detailed Description:

...or sufficient equivalent; and by assigning the OnEnter event or sufficient equivalent of the container object to a common process, most appropriately endowed to the governing CPO itself, which process looks up the corresponding 'cooperative resource descriptor" for the interface container,, and which process then assigns the "cooperative resource descriptor" to the focus of the CPO, therefore processes endowed...

22/3K/16 (Item 5 from file: 349) Links
Fulltext available through: Order File History
PCT FULLTEXT

00871028
METHOD AND APPARATUS FOR PROVIDING PROCESS-CONTAINER PLATFORMS
PROCEDE ET APPAREIL POUR LA CREATION DE PLATES-FORMES DE CONTENEURS DE PROCESSUS

Patent Applicant/Patent Assignee:

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(For all designated states except: US)

uu. FREED Erik J; *
US; US(Residence); US(Nationality)

Patent Applicant/Inventor:

vv. FREED Erik J
*; US; US(Residence); US(Nationality);

Legal Representative:

ww. SANTISI Steven(agent)
91 Bolivar Drive, Berkeley, CA 94710; US;

	Country	Number	Kind	Date
Patent	WO	200205119	A1	20020117
Application	WO	2001US21468		20010707
Priorities	US	2000216871		20000707

Designated States: (All protection types applied unless otherwise stated - for applications 2004+)

[EP] AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LU; MC; NL; PT; SE; TR;

[OA] BF; BJ; CF; CG; CI; CM; GA; GN; GW; ML; MR; NE; SN; TD; TG;

[AP] GH; GM; KE; LS; MW; MZ; SD; SL; SZ; TZ; UG; ZW;

[EA] AM; AZ; BY; KG; KZ; MD; RU; TJ; TM;

Main International Patent Classes (Version 7):

IPC	Level
G06F-017/00	Main

Publication Language: English
Filing Language: English
Fulltext word count: 28785

Detailed Description:

...Journaling
1 0 The Core Model has special hooks to support the concept of a Process-container Journal. This is done through supporting the appropriate event structure to provide hooks for any... ...Core Model's synchronization model is that al(inverted exclamation mark) documents and their contained objects are unshared. This means that the Core Model assumes, but does not enforce that there is only...data files, and non-XML documents.

Object resources
Many of the Resources contained within a Process-container represent documents that the Process-container Engine considers interpretable or non-opaque. These are mostly XIVIL documents, but inciude such files as Javascript and Cascading style sheets that are also 'understood' by the Process-container runtime as other than an opaque byte strearri. These interpreted Resources are converted to... ...properties of the understood object.

Meta-data Resources
Many of the Resources contained within a Process-container are considered 'meta-data'.

These meta-data Resources are read-orily, shared, and are expected to have matching content and identity from one Process-container to another. Meta-data defines the'type' of a Processcontainer.

Data Resources
Many of the Resources contalned within a Process-container are considered 'data'.

These data Resources are private to the Process-contalner, writeable, and are... ...content from one Process-contalner to another. Data is where the Instance' properties of
a Process-container are stored,
XCL Docurrients
Some of the content, in most cases Meta-data Resources, contain...uses three types of storage to capture the shared and non-shared state of a Process-container: Serialized Process-container, Serialized Journal, and/or Serialized Binders.

The Serialized Process-contalner is... ...separately from the Process-container and Journal because they are potentially shared resources across multiple Process- container instances.

The Store supports a set of types of indexing for Process-containers contained within (inverted exclamation mark)t.

Process-contalners are automatically accessible by specifying their identity using the Processcontalner's Resource VURL Resource. Process-containers are also accessible by Proc.esscontainer Variable. These are instances of XCL Variable placed within the body of the Processcontainer itseif. Other features inciude Process-container Management; Binder Management; DownIoading; Caching; Authentication, and Versioning.

13. DISTRIBUTION
The Process-container environment has a unique set of distribution chalienges and opportunities because of the asynchronous nature of Process-containers.

Process -container Mobillty
Process-containers are first of ali asynchronous self contalned portable agents. This 1 0 means that they...

NPL

17/5/1 (Item 1 from file: 2)
DIALOG(R)File 2: INSPEC

08387955 INSPEC Abstract Number: C2002-10-6150J-023
Title: Analysis of hierarchical fixed-priority scheduling
Author Saewong, S.; Rajkumar, R.; Lehoczky, J.P.; Klein, M.H.
Author Affiliation: Center for Design of Educ. Comput., Carnegie Mellon Univ., Pittsburgh, PA, USA
Conference Title: Proceedings 14th Euromicro Conference on Real-Time Systems. Euromicro RTS 2002 p. 173-81
Publisher: IEEE Comput. Soc , Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA x+265 pp.
ISBN: 0 7695 1665 3 Material Identity Number: XX-2002-02127
U.S. Copyright Clearance Center Code: 1068-3070/02/$17.00
Conference Title: Proceedings 14th Euromicro Conference on Real-Time Systems. Euromicro RTS 2002
Conference Date: 19-21 June 2002 Conference Location: Vienna, Austria

Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P)
Abstract: Reservation-based operating systems provide applications with guaranteed and timely access to system resources. One of their chief benefits is temporal isolation, which prevents the timing mis-behavior of one task from interfering with other tasks. Such a benefit is appealing enough for many systems (J.C. Bennett and H. Zhang, 1996) to recursively apply this reservation model to each of their components. This recursive application provides flexible load isolation among applications, users and other high-level resource management entities such as aggregated flows for network bandwidth. The hierarchical reservation study can be applied to hierarchical schedulers (Z. Deng and J.W.S. Liu, 1997), that support heterogenous scheduling algorithms. We propose and analyze a hierarchical reservation model in the context of fixed-priority scheduling, rate-monotonic and deadline-monotonic, as used in systems such as the Resource Kernel (R. Rajkumar et al., 1998). Detailed schedulability analyses under both deferrable-server and sporadic-server replenishment schemes, including exact completion time tests under hierarchical deadline-monotonic schedulers, are presented. We also derive the least upper scheduling bound for hierarchical rate-monotonic schedulers. Finally, we describe how to apply multi-reserve PCP (D. de Niz et al., 2001), an extension of the Priority Ceiling Protocol for reservation-based systems, to allow tasks to share nonpreemptable resources across the hierarchy. (15 Refs)
Subfile: C
Descriptors: operating systems (computers); real-time systems; resource allocation; scheduling
Identifiers: hierarchical fixed-priority scheduling; reservation-based operating systems ; system resources; temporal isolation; timing misbehavior; reservation model; recursive application; flexible load isolation; high-level resource management entities; aggregated flows; network bandwidth; hierarchical schedulers; hierarchical reservation model; fixed-priority scheduling; Resource Kernel; schedulability analyses; deferrable-server; sporadic-server replenishment schemes; exact completion time tests; hierarchical deadline-monotonic schedulers; upper scheduling bound; multi-reserve PCP; Priority Ceiling Protocol; nonpreemptable resource sharing; heterogenous scheduling algorithms
Class Codes: C6150J (Operating systems); C6150N (Distributed systems software)

17/5/2 (Item 2 from file: 2)
DIALOG(R)File 2: INSPEC

08014034 INSPEC Abstract Number: B2001-10-6135-009, C2001-10-1250-001
Title: Conflict detection during plan integration for multi-agent systems
Author Barber, K.S.; Liu, T.H.; Ramaswamy, S.
Author Affiliation: Dept. of Electr. & Comput. Eng., Texas Univ., Austin, TX, USA
Journal: IEEE Transactions on Systems, Man and Cybernetics, Part B (Cybernetics) vol.31, no.4 p. 616-28
Publisher: IEEE ,
Publication Date: Aug. 2001 Country of Publication: USA
CODEN: ITSCFI ISSN: 1083-4419
SICI: 1083-4419(200108)31:4L.616:CDDP;1-9
Material Identity Number: D488-2001-004
U.S. Copyright Clearance Center Code: 1083-4419/2001/$10.00
Document Number: S1083-4419(01)02503-1
Language: English Document Type: Journal Paper (JP)
Treatment: Applications (A); Practical (P)
Abstract: This paper describes techniques developed for conflict detection during plan integration. Agents' intensions are represented with intended goal structure (IGS) and the E-PERT diagrams. Conflicts are classified as goal, plan, and belief conflicts. Before integrating individual plans and detecting plan conflicts, agents first detect and eliminate their goal conflicts by exchanging their IGS. Plan integration is done through merging individual E-PERT diagrams. Project estimation and review technique (PERT) diagrams have been used extensively in the systems analysis area since the 1980s to provide a global consistent view of parallel activities within a project. We extended the PERT diagrams for use in the plan integration activity within multi-agent systems (MAS). The E-PERT diagram contributes to maintain traceable temporal relations among agents' local scheduled actions. Combined with pattern matching, plan conflicts due to resource sharing, or conflicting conditions (i.e., postconditions of one action disabling preconditions of another action) can be detected. The conflict detection techniques are implemented in a sensible agent testbed to promote deployment and performance analysis. (27 Refs)
Subfile: B C
Descriptors: belief maintenance; multi-agent systems; pattern matching; performance evaluation; PERT; systems analysis
Identifiers: conflict detection; plan integration; multi-agent systems; intended goal structure; belief conflicts; E-PERT diagrams; project estimation and review technique; systems analysis; plan integration activity; traceable temporal relations; local scheduled actions; pattern matching; resource sharing; conflicting conditions; performance analysis
Class Codes: B6135 (Optical, image and video signal processing); C1250 (Pattern recognition); C6170K (Knowledge engineering techniques); C1230R (Reasoning and inference in AI); C5470 (Performance evaluation and testing); C6170 (Expert systems and other AI software and techniques)

17/5/7 (Item 7 from file: 2)
DIALOG(R)File 2: INSPEC

06637793 INSPEC Abstract Number: C9708-4240P-051
Title: An efficient algorithm for finding all maximal conflict sets in concurrent programs
Author Hiraishi, K.
Author Affiliation: Adv. Inst. of Sci. & Technol., Ishikawa, Japan
Conference Title: Proceedings. Second International Workshop on Software Engineering for Parallel and Distributed Systems (Cat. No.97TB100154) p. 39-47
Publisher: IEEE Comput. Soc , Los Alamitos, CA, USA
Publication Date: 1997 Country of Publication: USA x+311 pp.
ISBN: 0 8186 8043 1 Material Identity Number: XX97-01582
U.S. Copyright Clearance Center Code: 0 8186 8043 1/97/$10.00
Conference Title: Proceedings of PDSE '97: 2nd International Workshop on Software Engineering for Parallel and Distributed Systems
Conference Sponsor: ACM SIGSOFT; IEEE Comput. Soc.; IFIP
Conference Date: 17-18 May 1997 Conference Location: Boston, MA, USA

Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Conflict is one of the fundamental situations that appear in concurrent programs. Conflict occurs when more than one processes share common resources. An occurrence of the action of one process disables actions of other processes which are in conflict. Controlling conflicts is very important in concurrent programming, especially for rule-based programming. We can find all conflicts by generating the state space, but largeness of the state space make this difficult. In this paper, we show an efficient algorithm to find all maximal conflict sets in concurrent programs. The proposed algorithm is based on partial order methods, and generates a reduced state space that preserves all maximal conflict sets. (13 Refs)
Subfile: C
Descriptors: concurrency control; finite automata; parallel programming; programming theory; resource allocation
Identifiers: maximal conflict set finding; concurrent program conflicts; common resource sharing; concurrent programming; rule-based programming; state space generation; partial order methods; finite state automata; concurrency control; deadlocks
Class Codes: C4240P (Parallel programming and algorithm theory); C6110P (Parallel programming); C6150N (Distributed systems software); C4220 (Automata theory)

17/5/8 (Item 8 from file: 2)
DIALOG(R)File 2: INSPEC

06429931 INSPEC Abstract Number: C9701-4240P-009
Title: Local coteries and a distributed resource allocation algorithm
Author Kakugawa, H.; Yamashita, M.
Author Affiliation: Fac. of Eng., Hiroshima Univ., Japan
Journal: Transactions of the Information Processing Society of Japan vol.37, no.8 p. 1487-96
Publisher: Inf. Process. Soc. Japan ,
Publication Date: Aug. 1996 Country of Publication: Japan
CODEN: JSGRD5 ISSN: 0387-5806
SICI: 0387-5806(199608)37:8L.1487:LCDR;1-1
Material Identity Number: T205-96011

Language: Japanese Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: We discuss a resource allocation problem in distributed systems. Consider a distributed system consisting of a set of processes and a set of resources of identical type. Each process has access to a (sub)set of the resources. Different processes may have access to different sets of the resources. Each resource must be accessed in a mutually exclusive manner, and processes are allowed to request more than one resource at a time. Since all resources are of identical type, a process requesting k resources does not insist on k particular resources. However, once a resource has been allocated to a process, it cannot be allocated to another process until it is released. The mutual exclusion and k-mutual exclusion problems can be considered as special cases of the resource allocation problem. We first introduce a new class of quorum sets named local coteries as an extension of coteries, to take advantages of the fact that, in general, resources are not shared by all processes. Then, we propose a resource allocation algorithm, using a local coterie, that is both deadlock- and starvation-free. This algorithm allows resources requested by two processes to be allocated without any interference . (18 Refs)
Subfile: C
Descriptors: communication complexity; concurrency control; distributed algorithms; graph theory; resource allocation
Identifiers: local coteries; distributed resource allocation algorithm; distributed systems; message complexity; identical type resources; mutual exclusion; quorum sets; deadlock-free; starvation-free
Class Codes: C4240P (Parallel programming and algorithm theory); C6150N (Distributed systems software); C1160 (Combinatorial mathematics)

17/5/9 (Item 9 from file: 2)
DIALOG(R)File 2: INSPEC

06294878 INSPEC Abstract Number: C9607-4240C-054
Title: Contention-free complexity of shared memory algorithms
Author Alur, R.; Taubenfeld, G.
Author Affiliation: AT&T Bell Labs., Murray Hill, NJ, USA
Journal: Information and Computation vol.126, no.1 p. 62-73
Publisher: Academic Press ,
Publication Date: 10 April 1996 Country of Publication: USA
CODEN: INFCEC ISSN: 0890-5401
SICI: 0890-5401(19960410)126:1L.62:CFCS;1-G
Material Identity Number: K729-96005
U.S. Copyright Clearance Center Code: 0890-5401/96/$18.00

Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Worst-case time complexity is a measure of the maximum time needed to solve a problem over all runs. Contention-free time complexity indicates the maximum time needed when a process executes by itself, without competition from other processes. Since contention is rare in well-designed systems, it is important to design algorithms which perform well in the absence of contention. We study the contention-free time complexity of shared memory algorithms using two measures: step complexity, which counts the number of accesses to shared registers; and register complexity, which measures the number of different registers accessed. Depending on the system architecture, one of the two measures more accurately reflects the elapsed time. We provide lower and upper bounds for the contention-free step and register complexity of solving the mutual exclusion problem as a function of the number of processes and the size of the largest register that can be accessed in one atomic step. We also present bounds on the worst-case and contention-free step and register complexities of solving the naming problem. These bounds illustrate that the proposed complexity measures are useful in differentiating among the computational powers of different primitives. (16 Refs)
Subfile: C
Descriptors: computational complexity; naming services; shared memory systems
Identifiers: contention-free complexity; shared memory algorithms; worst-case time complexity; step complexity; register complexity; system architecture; mutual exclusion problem; naming problem
Class Codes: C4240C (Computational complexity); C6120 (File organisation); C5440 (Multiprocessing systems)

17/5/10 (Item 10 from file: 2)
DIALOG(R)File 2: INSPEC

06202283 INSPEC Abstract Number: C9604-6110P-036
Title: Distributed shared abstractions (DSA) on multiprocessors
Author Clemencon, C.; Mukherjee, B.; Schwan, K.
Author Affiliation: Integrated Syst. Eng. AG, Zurich, Switzerland
Journal: IEEE Transactions on Software Engineering vol.22, no.2 p. 132-52
Publisher: IEEE ,
Publication Date: Feb. 1996 Country of Publication: USA
CODEN: IESEDJ ISSN: 0098-5589
SICI: 0098-5589(199602)22:2L.132:DSAM;1-Y
Material Identity Number: I271-96002

Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P)
Abstract: Any parallel program has abstractions that are shared by the program`s multiple processes. Such shared abstractions can considerably affect the performance of parallel programs, on both distributed and shared memory multiprocessors. As a result, their implementation must be efficient, and such efficiency should be achieved without unduly compromising program portability and maintainability. The primary contribution of the DSA library is its representation of shared abstractions as objects that may be internally distributed across different nodes of a parallel machine. Such distributed shared abstractions (DSA) are encapsulated so that their implementations are easily changed while maintaining program portability across parallel architectures. The principal results presented are: a demonstration that the fragmentation of object state across different nodes of a multiprocessor machine can significantly improve program performance; and that such object fragmentation can be achieved without compromising portability by changing object interfaces. These results are demonstrated using implementations of the DSA library on several medium scale multiprocessors, including the BBN Butterfly, Kendall Square Research, and SGI shared memory multiprocessors. The DSA library`s evaluation uses synthetic workloads and a parallel implementation of a branch and bound algorithm for solving the traveling salesperson problem (TSP). (46 Refs)
Subfile: C
Descriptors: data structures; distributed memory systems; parallel architectures; parallel machines; parallel programming; software maintenance; software portability
Identifiers: distributed shared abstractions; multiprocessors; parallel program; shared memory multiprocessors; parallel architectures; maintainability; DSA library; internally distributed; parallel machine; program portability; object state; multiprocessor machine; object interfaces; medium scale multiprocessors; BBN Butterfly; Kendall Square Research; SGI shared memory multiprocessors; synthetic workloads; parallel implementation; branch and bound algorithm; traveling salesperson problem
Class Codes: C6110P (Parallel programming); C5440 (Multiprocessing systems); C5220P (Parallel architecture); C6120 (File organisation); C6110B (Software engineering techniques)

17/5/11 (Item 11 from file: 2)
DIALOG(R)File 2: INSPEC

06083782 INSPEC Abstract Number: C9512-1290-002
Title: Allocation sequences of two processes sharing a resource
Author Gaujal, B.; Jafari, M.; Baykal-Gursoy, M.; Alpan, G.
Author Affiliation: Dimacs Center, Rutgers Univ., Piscataway, NJ, USA
Journal: IEEE Transactions on Robotics and Automation vol.11, no.5 p. 748-53

Publication Date: Oct. 1995 Country of Publication: USA
CODEN: IRAUEZ ISSN: 1042-296X
U.S. Copyright Clearance Center Code: 1042-296X/95/$04.00

Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: We study a Petri net model of a system composed of two processes sharing a resource. Conflicts may occur over the usage of the shared resource, thus making the system nondeterministic. Therefore, in the context of minimax algebra, it cannot be formulated as a linear system in order to compute its performance measures. However, if the sequence by which the resource is allocated to the two processes is known, we can transform the system into a decision-free net. For this system with an imposed constraint on the resource allocation frequencies, we show that the optimal allocation sequence is the most regular integer sequence satisfying that constraint. We also discuss the periodic behavior of this system under no constraints on the resource allocation frequencies. (10 Refs)
Subfile: C
Descriptors: discrete event systems; minimax techniques; operations research; Petri nets ; resource allocation
Identifiers: resource sharing; Petri net model; nondeterministic systems; minimax algebra; resource allocation; decision-free net; optimal allocation sequence
Class Codes: C1290 (Applications of systems theory); C1180 (Optimisation techniques); C1160 (Combinatorial mathematics)

17/5/12 (Item 12 from file: 2)
DIALOG(R)File 2: INSPEC

06016119 INSPEC Abstract Number: C9509-4240P-065
Title: A fault-tolerant dynamic resource allocation algorithm
Author Injong Rhee
Author Affiliation: Dept. of Comput. Sci., North Carolina Univ., Chapel Hill, NC, USA
Conference Title: Proceedings of the Thirteenth Annual ACM Symposium on Principles of Distributed Computing p. 380
Publisher: ACM , New York, NY, USA
Publication Date: 1994 Country of Publication: USA ix+406 pp.
ISBN: 0 89791 654 9
U.S. Copyright Clearance Center Code: 0 89791 654 9/94/0008.$3.50
Conference Title: Proceeding of 13th ACM Symposium on Principles of Distributed Computing
Conference Sponsor: ACM
Conference Date: 14-17 Aug. 1994 Conference Location: Los Angeles, CA, USA

Language: English Document Type: Conference Paper (PA)
Treatment: Theoretical (T)
Abstract: Distributed systems commonly include resources (CPUs, I/O channels, buffer space, data files, etc.) which must be managed so that no two conflicting processes with overlapping resource requirements access the resources at the same time, while avoiding starved or deadlocked processes. The scheduling of processes with various resource requirements in this type of system is generally known as resource allocation. The dynamic resource allocation problem models resource allocation in a dynamic system where processes with various resource requirements can be dynamically created and terminated, and therefore, processes have no a priori knowledge about their conflicting processes. An asynchronous distributed message passing system is assumed. We present a dynamic resource allocation algorithm with the optimal failure locality. The worst case response time of this algorithm is O(n), where n is the total number of processes in the system, assuming the message delay and the time duration that a process is in the critical region are some constants. This is the first work that explicitly considers the failure locality in a dynamic system. In our algorithm, the priorities of processes in accessing resources are determined dynamically using time stamps. A process holds resources only when they are certain to acquire all its required resources. This way, low priority processes can make progress despite possible failure of high priority processes. (2 Refs)
Subfile: C
Descriptors: computational complexity; distributed algorithms; fault tolerant computing; message passing; processor scheduling; resource allocation
Identifiers: fault-tolerant dynamic resource allocation algorithm; distributed systems; overlapping resource requirements; process scheduling; asynchronous distributed message passing system; optimal failure locality; worst case response time; message delay; time duration; critical region; failure locality; process priorities; time stamps; high priority processes; low priority processes
Class Codes: C4240P (Parallel programming and algorithm theory); C6150N (Distributed systems software); C4240C (Computational complexity); C6110 (Systems analysis and programming); C5470 (Performance evaluation and testing)

17/5/14 (Item 14 from file: 2)
DIALOG(R)File 2: INSPEC

05062727 INSPEC Abstract Number: C9202-5220P-106
Title: Deadlock handling methods for pipeline concurrently flowing processes
Author Wojcik, R.; Banaszak, Z.
Author Affiliation: Inst. of Tech. Eng., Wrocklaw Tech. Univ., Poland
Journal: Prace Naukowe Instytutu Cybernetyki Technicznej Politechniki Wroclawskiej, Seria: Konferencje no.39 p. 53-8

Publication Date: 1991 Country of Publication: Poland
CODEN: PICWDU ISSN: 0324-9794

Language: English Document Type: Journal Paper (JP)
Treatment: Practical (P); Theoretical (T)
Abstract: Multiple-resource-per-operation processes with competition for access to a shared resource system are considered. An overview of deadlock handling methods for pipeline-like processes is presented. (8 Refs)
Subfile: C
Descriptors: concurrency control; pipeline processing
Identifiers: multiple-resource-per-operation processes; system resource sharing; pipeline concurrently flowing processes; deadlock handling methods
Class Codes: C5220P (Parallel architecture); C5440 (Multiprocessor systems and techniques); C6150N (Distributed systems)

17/5/15 (Item 15 from file: 2)
DIALOG(R)File 2: INSPEC

01641908 INSPEC Abstract Number: C74013576
Title: On the memory conflict problem in multiprocessor systems
Author Kurtzberg, J.M.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Transactions on Computers vol.C-23, no.3 p. 286-93

Publication Date: March 1974 Country of Publication: USA
CODEN: ITCOB4 ISSN: 0018-9340

Language: English Document Type: Journal Paper (JP)
Treatment: Theoretical (T)
Abstract: This paper presents quadratic programming models of memory conflict in multiprocessor systems where main memory consists of a set of memory modules common to all processors. Two jobs (programs) are said to be in conflict, or subject to memory conflict, whenever at a given time portions of them must be executed in the same memory module by different processors. One is interested in minimizing the total conflict by the proper assignment of jobs to main memory. Two allocation models are considered: one in which the jobs-to-memory assignment is to be made independent of any particular processors-to-jobs schedule, that is, expected memory conflict is to be minimized over the space of all schedules; and the second in which a definite processor schedule is assumed to be available. For both models, algorithms are formulated for the assignment of jobs to memory. (11 Refs)
Subfile: C
Descriptors: multiprocessing programs; quadratic programming; storage allocation
Identifiers: allocation model; computer slowdown; feasible allocation; assignment; memory conflict; multiprocessor systems; quadratic programming model; shared storage environment; storage allocation algorithms; storage interference; storage lockout
Class Codes: C6120 (File organisation); C6150J (Operating systems)

17/5/17 (Item 2 from file: 6)
DIALOG(R)File 6: NTIS

1272341 NTIS Accession Number: AD-A173 283/3
Applying Activation Theory for Modeling Task Interference in Dual-Task Situations
(Final rept. Mar 85-Jun 86)
Navon, D.
California Univ., San Diego, La Jolla. Inst. for Cognitive Science.
Corporate Source Codes: 005436056; 413706

14 Jun 86 14p
Language: English
Journal Announcement: GRAI8703
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A02/MF A01
Country of Publication: United States
Contract Number: N00014-85-K-0313; RR04206; RR04206OA
The purpose of this one-year contract was to attempt to model the sources of task interference other than competition for processing resources. First, a general theory of attention was developed. The theory posits parallel computations by entities called modules, with little competition for common resources. Attention is assumed to control only the communication among modules. It is shown that the attentional mechanism is a vehicle for achieving selectivity, but is less fit for coping with multiple goals. Second, task interference of a type that is called crosstalk was computer-simulated on a parallel distributed processing network. Several interesting results emerge out of the simulation. Third, the role of conflict between outcomes of processes in producing task interference was studied experimentally. Subjects searched for different sorts of targets, each assigned to a different attentional channel. Confusability between channels and congruence of responses to them were found to be potent determinants of task interference. The author suggest that potential sources of outcome conflict may contribute to dual-task interference and argue that a great deal of the residual interference might result from other sorts of outcome conflict.
Descriptors: *Interference; *Attention; Performance(Human); Computerized simulation; Activation; Computations; Conflict; Crosstalk; Distributed data processing; Models; Networks; Parallel processing; Processing; Residuals; Resources; Roles(Behavior); Simulation; Sources; Theory; Targets
Identifiers: Task Interference; Dual Tasks; NTISDODXA
Section Headings: 92B (Behavior and Society--Psychology)

1165641 NTIS Accession Number: AD-A150 985/0
Effect of Strategy in Second Order Manual Control on Resource Competition with a Sternberg Memory Search Task
(Technical rept)
Goettl, B. P. ; Wickens, C. D.
Illinois Univ. at Urbana-Champaign. Engineering-Psychology Research Lab.
Corporate Source Codes: 034597127; 410871
Report Number: EPL-84-3/ONR-84-2
Mar 84 41p
Language: English
Journal Announcement: GRAI8511
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: United States
Contract Number: N00014-79-C-0658
This study examines the effects of two different strategies of second order manual control performance on dual-task interference using the multiple resources framework. A 'response-strategy' involves discrete time-optimal double impulse control based on momentary error. A perceptual strategy involves continuous control based upon momentary error velocity. Subjects can obtain equal levels of single task performance on both tasks. Each strategy is then time-shared with a Sternberg Memory Search task, which uses either spatial or visual material and is displayed either auditorily or visually. Two different biases of resource allocation between the two tasks are also included. An additional manipulation was task emphasis. In different conditions subjects are requested to emphasize tracking on the Sternberg task. The results indicated that performance using the response strategy showed a greater effect of changes in the Sternberg task code and modality than did performance using the perceptual strategy. Benefits in dual-task performance were realized with the auditory display when in double impulse, but not the continuous strategy, was employed.
Descriptors: *Response; *Performance(Human); *Memory(Psychology); Strategy; Searching
Identifiers: Sternberg task; NTISDODXA
Section Headings: 92B (Behavior and Society--Psychology)

17/5/21 (Item 6 from file: 6)
DIALOG(R)File 6: NTIS

0890545 NTIS Accession Number: AD-A097 235/6/XAB
Different Difficulty Manipulations Interact Differently with Task Emphasis: Evidence for Multiple Resources
(Interim rept. 1 Oct 78-30 Sep 79)
Gopher, D. ; Brikner, M. ; Navon, D.
Technion - Israel Inst. of Tech., Haifa. Center of Human Engineering and Industrial Safey Research.
Corporate Source Codes: 016872017; 412261
Sponsor: Air Force Office of Scientific Research, Bolling AFB, DC.
Report Number: HEIS-79-27; AFOSR-TR-81-0292
Feb 80 34p
Language: English
Journal Announcement: GRAI8116
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01
Country of Publication: Israel
Contract Number: AFOSR-77-3131; 2313; A2
A two-dimensional pursuit tracking task was paired with three variants of a letter typing task to test predictions about the effects of task difficulty and task emphasis derived from a model of multiple resources, which states that tasks can overlap to various degrees in their demand for resources. Under dual-task conditions, when difficulty and priorities of tasks are jointly manipulated, difficulty parameters that tap processing resources shared by both tasks interact with priorities, while parameters that are relevant to one task only have additive effects on performance. In the present experiment a fixed difficulty tracking task was paired with a letter typing task on which difficulty was manipulated by varying cognitive or motor factors. In addition, task priorties were manipulated and the instantaneous difference between actual and desired performance was continuously displayed to the subjects. Task priority in dual-task conditions had large effect on the performance of the two tasks suggesting the existence of competition for resources. Both types of difficulty manipulations had large effects on performance. However, only motor difficulty interacted with priorites. The results are interpreted to indicate that joint performance of typing and tracking mainly complete for motor-related resources, while the size of the stimulus set tap a separate resource which is primarily relevant to the letter typing task. (Author)
Descriptors: *Tracking; *Predictions; *Performance tests; Motor reactions; Two dimensional; Models; Interactions; Test methods; Reaction time; Perception(Psychology); Stimuli; Israel
Identifiers: NTISDODXA; NTISDODAF
Section Headings: 95D (Biomedical Technology and Human Factors Engineering--Human Factors Engineering)

17/5/24 (Item 2 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)

06576000 E.I. Monthly No: EIM9303-016113
Title: Does secondary task measure outcome conflict or resource allocation?.

Author: Tsang, Pamela S.; Shaner, Tonya L.
Corporate Source: Wright State Univ, Dayton, OH, USA
Conference Title: Proceedings of the Human Factors Society 36th Annual Meeting. Part 2 (of 2)
Conference Location: Atlanta, GA, USA Conference Date: 19921012
E.I. Conference No.: 17554
Source: Proceedings of the Human Factors Society v 2. Publ by Human Factors Soc Inc, Santa Monica, CA, USA. p 1398-1402
Publication Year: 1992
CODEN: PHFSDQ ISSN: 0163-5182
Language: English
Document Type: PA; (Conference Paper) Treatment: X; (Experimental)
Journal Announcement: 9303
Abstract: The secondary task technique was used to test two alternative explanations of dual task decrement: outcome conflict and resource allocation. Subjects time-shared a continuous tracking task and a discrete Sternberg memory task. The memory probes were presented under three temporal predictability conditions. Dual task performance decrements in both the tracking and memory tasks suggested that the two tasks competed for some common resources, processes, or mechanisms. Although performance decrements were consistent with both the outcome conflict and resource allocation explanations, the two explanations propose different mechanisms by which the primary task could be protected from interference from the concurrent secondary task. The primary task performance could be protected by resource allocation or by strategic sequencing of the processing of the two tasks in order to avoid outcome conflict. In addition to examining the global trial means, moment-by-moment tracking error time-locked to the memory probe was also analyzed. There was little indication that the primary task was protected by resequencing of the processing of the two tasks. This together with the suggestion that predictable memory probes led to better protected primary task performance than less predictable memory probes lend support for the resource explanation. (Author abstract) 4 Refs.
Descriptors: *HUMAN ENGINEERING; MANUAL CONTROL; OPERATIONS RESEARCH; SUBJECTIVE TESTING
Identifiers: TRACKING TASK; DUAL TASK DECREMENT; RESOURCE ALLOCATION; PERFORMANCE DECREMENT; OUTCOME CONFLICT
Classification Codes:
461 (Biotechnology); 912 (Industrial Engineering & Management)
46 (BIOENGINEERING); 91 (ENGINEERING MANAGEMENT)

17/5/25 (Item 3 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)

03122663 E.I. Monthly No: EI71X009170
Title: Sequencing tasks in multiprocess systems to avoid deadlocks.

Author: SHOSHANI, A.; COFFMAN, E. G.
Corporate Source: System Develop Corp, Santa Monica, Calif
Source: IEEE Conf Rec 1970 11th Annu Symp on Switching & Automata Theory, Santa Monica, Calif, Oct 28-30 1970 p 225-35
Publication Year: 1970
Language: ENGLISH
Journal Announcement: 71X0
Abstract: The "deadlock" problem may occur in a system in which resources are shared among users. Deadlock is a situation in which two or more jobs cannot be completed because of conflicting resource requirements. In this paper, it is assumed that advance information about future resource requirements of jobs is available. In particular, it is assumed that jobs are represented as a sequence of "job steps" during which the resource usage remains constant. An algorithm which uses this information to determine whether a request can be granted without causing a deadlock is presented.
Descriptors: *AUTOMATA THEORY; COMPUTERS--Data Processing
Identifiers: COMPUTER THEORY; MULTIPROCESSING SYSTEMS
Classification Codes:
721 (Computer Circuits & Logic Elements); 723 (Computer Software)
72 (COMPUTERS & DATA PROCESSING)

17/5/27 (Item 2 from file: 34)
DIALOG(R)File 34: SciSearch(R) Cited Ref Sci

07165624 Genuine Article#: 131TK Number of References: 55
Concurrent performance of two working memory tasks: Potential mechanisms of interference

Author: Klingberg T (REPRINT)
Corporate Source: KAROLINSKA INST,DIV HUMAN BRAIN RES, DEPT NEUROSCI, DOKTORSRINGEN 12/S-17177 STOCKHOLM//SWEDEN/ (REPRINT)
Journal: CEREBRAL CORTEX , 1998 , V 8 , N7 (OCT-NOV) , P 593-601
ISSN: 1047-3211 Publication date: 19981000
Publisher: OXFORD UNIV PRESS INC , JOURNALS DEPT, 2001 EVANS RD, CARY, NC 27513
Language: English Document Type: ARTICLE
Geographic Location: SWEDEN
Subfile: CC LIFE--Current Contents, Life Sciences;
Journal Subject Category: NEUROSCIENCES
Abstract: When two tasks are performed simultaneously, performance often deteriorates, with concomitant increases in reaction time and error rate. Three potential neurophysiological mechanisms behind this deterioration in performance have been considered here: (i) dual-task performance requires additional cognitive operations and activation of cortical areas in addition to those active during single-task performance; (ii) two tasks interfere if they require activation of the same part of cortex; and (iii) cross-modal inhibition causes interference between two tasks involving stimuli from different sensory modalities. Positron emission tomography was used to measure regional cerebral blood flow (rCBF) during performance of an auditory working memory (WM) task, a visual WM task, both WM tasks (dual task) and a control condition. Compared to the control condition, the auditory and visual WM tasks activated sensory-specific areas in the superior temporal gyrus and occipital pole respectively. Both WM tasks also activated overlapping parts of cortex in the dorsolateral prefrontal, inferior parietal and cingulate cortex. There was no separate cortical area which was activated only in the dual task, and thus no area which could be associated with any dual task specific cognitive process such as task-coordination or divided attention. Decrease in rCBF in one WM task did not overlap with the areas of rCBF increase in the other WM task. However, an inhibitory mechanism could not be ruled out, since the rCBF increase in sensory specific areas was smaller in the dual-task condition than in the single-task conditions. The cortical activity underlying WM was to a large extent organized in a non-sensory specific, or non-parallel, way, and the results are consistent with the hypothesis that concurrent tasks interfere with each other if they demand activation of the same part of cortex.
Identifiers-- KeyWord Plus(R): POSITRON-EMISSION TOMOGRAPHY; DORSOLATERAL PREFRONTAL CORTEX; HUMAN EXTRASTRIATE CORTEX; TIME-SHARING ABILITY; SHORT-TERM- MEMORY; SOMATOSENSORY CORTEX; DIVIDED ATTENTION; ACTIVATION; PET; OBJECT
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17/5/30 (Item 5 from file: 34)
DIALOG(R)File 34: SciSearch(R) Cited Ref Sci

03555011 Genuine Article#: PM289 Number of References: 8
A REAL-TIME SCHEDULING ALGORITHM FOR TASKS WITH RESOURCE CONTENTION ON A MULTIPROCESSOR

Author: RYANG DS; PARK KH
Corporate Source: KAIST,DEPT ELECT ENGN,373-1 KUSONG DONG/TAEJON//SOUTH KOREA/
Journal: JOURNAL OF CIRCUITS SYSTEMS AND COMPUTERS , 1994 , V 4 , N3 (SEP) , P 243-253
ISSN: 0218-1266
Language: ENGLISH Document Type: ARTICLE
Geographic Location: SOUTH KOREA
Subfile: SciSearch
Journal Subject Category: ENGINEERING, ELECTRICAL & ELECTRONIC; COMPUTER SCIENCE, HARDWARE & ARCHITECTURE
Abstract: Our scheduling algorithm is based on a general model with timing and resource constraints which permits OR requests. In order to keep run-time costs low, we propose an algorithm that does not search the whole search space. This paper defines two measures, survivability and impact, for scheduling tasks conflicted for some resources. The survivability is a metric to show how urgent a task is, and how constrained it is by its resources. The impact of a resource for a task measures how much other tasks are influenced by the allocation of the resource to the task. Our scheduling algorithm uses the survivability to schedule tasks on multiple processors. After a task is picked out to be run in a time slice using the survivability, the least impact resources are allocated from several alternative resources.
Research Fronts: 92-0144 002 (PERFORMANCE EVALUATION OF PARALLEL SYSTEMS; LARGE-SCALE SHARED-MEMORY MULTIPROCESSORS; PETRI NET BASED MODEL; VLSI COMMUNICATION SWITCHES; CONSTANT FACTOR)
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INTERFERENCE BETWEEN SWITCHED TASKS

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Abstract: Interference between tasks in a task-switching situation was interpreted in terms of theoretical models of time-sharing. Controlled processing of two separate tasks in a time-sharing situation was hypothesized to require a strategy of management whose ease of execution depends on the complexity of the task involved- Switching from one task to the other requires activation of the resources required for performance of the new task and inhibition of the resources engaged in the first task. Failures in either of these two processes will interfere with the performance of the second task. This hypothesis was tested in a situation in which subjects had to switch from one detection task to another. Interruption of one task to carry out another task increased both processing time and error rate in the second task. The types of error (intrusions, confusions and omissions) were considered to be specific to time-sharing.
Descriptors--Author Keywords: TIME-SHARING; INTERFERENCE; RESOURCES; DUAL TASKS
Identifiers-- KeyWords Plus: INDIVIDUAL-DIFFERENCES; MULTIPLE RESOURCES; ATTENTION; PERFORMANCE
Research Fronts: 90-0891 006 (IMPLICIT MEMORY; AUTOMATIC PROCESSING; MODEL FOR UNDERSTANDING COGNITIVE DISTURBANCES)
90-7853 001 (MENTAL MODELS; INTERFACE DESIGN; TRAFFIC BEHAVIOR; RESOURCE AVAILABILITY)
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THE GENERALIZED MUTUAL EXCLUSION PROBLEM IN A COMPUTER SYSTEM

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In most computer systems processes compete with each other by requesting and holding resources exclusively. In addition, processes may cooperate by planned interactions involving shared data or by message passing. In either case mutual exclusion with respect to certain information or resources is necessary. We must ensure that only one process at a time holds a resource or modifies shared information.

The problem of how to implement mutual exclusion has been studied extensively. There are many existing solutions which are designed either for 1 of N mutual exclusion or for special classes of the mutual exclusion problem. These solutions are all associated with some constraints and behavioral characteristics. It is not clear which constraints are inherent in the problems themselves and which are due to the synchronization mechanism employed. In this dissertation, we consider the limitations of mutual exclusion problem and synchronization mechanisms in both shared memory and distributed systems. We also consider various new methods of implementing the required synchronization for a generalized class of mutual exclusion problems.

A model, called the ME-graph model, is used to describe the mutual exclusion problem here. We analyze some common behavioral characteristics possessed in the mutual exclusion problem such as usually essential requirements, efficiency considerations, and symmetry considerations. We show that some of these characteristics are contradictory but some of them are congenial.

We introduce five new methods with different approaches to solve the mutual exclusion problem. They are all built on the ME-graph model and therefore can solve a more general class of mutual exclusion problems than previous solutions. They also can be used to solve resource allocation problems. These new solutions are all free from deadlock and starvation.

The first two solutions are based on the same idea. One of them is implemented by binary semaphores and the other uses message passing. The advantage of these two solutions is that they require fewer system resources, such as semaphores and messages, than other solutions. They also reduce the length of max-waiting chain to $\vert$C$\vert$, where $\vert$C$\vert$ is the number of colors needed for edge coloring of the ME-graph.

The third solution employs a global queue managed by an additional queue manager process. The contribution of this solution is that the length of waiting chains is at most 2. This length is optimal and much smaller than that of previous solutions. Our next solution replaces the global queue by a number of virtual queues. All waiting chains also have length at most 2. These two solutions are implemented with messages.

The last solution also gives minimal-length waiting chains but uses centralized synchronization based on semaphores.